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A REVIEW OF 3.3- 5 GHz CMOS LNA USING DIFFERENT TOPOLOGIES

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ABSTRACT

This paper presents the literature review of designing LNA using different topol-ogies. Designing very high-performance LNAs is an active research area and is of crucial importance for wireless technologies. Most important parameters considered in any LNA are Gain,Noise figure, Linearity and Input Output impedance Matching.

KEYWORDS: Low noise amplifier,Common Gate Source,Noise Figure, Impedance matching, High gain.

INTRODUCTION

Low noise amplifier is a key component of receiver in radio communication systems. The main function of LNA is to provide high gain and minimum noise figure to successive modules of receiver for best performance. A number of designs of LNA are presented in literature by using different topologies and techniques. This paper presents brief review of the research done by various researchers in the area of designing of LNA for 3.3 GHz to 5 GHz range of frequency. current reuse, cascade amplifiers, cascoded amplifiers topology, source degeneration topology, resistive feedback, cross coupled capacitor technique, g_m −boosted current reuse topology, single stage, multistage designs are the techniques, that are used for designing LNA. One of the most efficient technique is inductive degeneration because it provides resistive component and reduces power dissipation. CMOS LNA architectures can be divided into two major groups the common source and the common gate LNA **.**

STUDY OF EXISTING TECHNIQUES

To begin some work first we need to analyse and study the work done in past by the researchers of the specific field,so that we can understand the concepts and recent techniques . This paper presents a brief review of the researchs done in past by different researchers in the area of designing of LNA by simple current reuse, cascade amplifiers, cascoded amplifiers topology, source degeneration topology, resistive feedback, g_m −boosted current reuse topology, single stage, differential,multistage designs which are the best design techniques. It is very essential to keep high gain with linearity and a low noise figure. The following literature review discusses all the above techniques.
In following literature review we'll discusses the techniques for desiging the LNA.

Hyung-Jin Lee, Dong S. Ha, Sang S. Choi (2006) proposed a 3 to 5 GHz CMOS UWB LNA with Input Matching using Miller Effect. They used chebyshev filter for input matching and a source follower for output matching which provide low power consumption. The measured power gain of LNA is above 15dB over the frequency range of interest. The overall NF is lower than 2.3dB., S_{11} is less than -10.5dB, S_{22} is less than -13.1dB. This proposed LNA core draws 6.4mA from a of 1.2V power supply. [1]

Yu-Cheng Hsu, Ping-Hsun Wu, Cheng-Chung Chen, Jian-Yu Li, Sheng-Feng Lee, Wu-Jing Ho and Cheng-Kuo Lin (2007) proposed a Single-chip RF Front-end MMIC using InGaAs E/DpHEMT for 3.5 GHz WiMAX Applications. In this paper, D-pHEMT was applied for switch designed and E-pHEMT was applied for LNA and PA design. The proposed schematic of LNA provides NF of 1.8 dB,gain of 16.5dB,-10dBm of input P1dB and 3 dBm of

IIP3.The SPDT results are 0.8 dB of insertion loss, 20 dB of isolation and 27.4 dBm of input P1dB. E/D-pHEMT technology for the RF front-end cause low cost, small size and easy integration. [2]

M. Ben Amor, M. Loulou, S. Quintanel and D. Pasquet (2008) proposed a wideband CMOS LNA design for WiMAX applications. LNA cover the frequency range 2.3 to 5.9 GHz for licensed and unlicensed bands of the WiMAX. S_{11} and S_{22} lower than -10dB, a gain of 13dB and a noise figure between 3 dB for all the band. They used chebyshev filter in input matching and an inductive shunt feedback for output matching.the current induced is of 25mA and supply voltage is of 2.5v.[3]

Jouni Kaukovuori , Mikko Kaltiokallio and Jussi Ryynanen (2008) proposed the design of a CG LNA for the wideband applications. Effect of the different components for wideband input matching along with effect of the matching network on the linearity and noise of a CG stage was analyzed. [4]

S.k Wrong, F.Kung Wai Lee, S.Maisurah, M.N.B.Osman and S.J.Hui (2009) proposed the design of 3 to 5 GHz CMOS LNA for UWB System. This LNA employing interstage matching inductor on conventional cascade inductive source degeneration structure. The proposed LNA is implemented in 0.18μm CMOS technology.Interstage inductor which is used in this LNA can increase the overall broadband gain and suppress the noise figure. The measured power gain is +12.7dB, S_{11} is 18dB, S_{22} is 3dB, NF of 4.5dB. It dissipate 17mw of power from 1.8V supply voltage.[5]

Jaewoo Park, Shin-Nyoung Kim, Yong-Seong Roh, and Changsik Yoo (2010) proposed a CMOS direct-conversion receiver by employing a voltage feedback in a common-gate low-noise amplifier (LNA). In the proposed schematic the input matching of the LNA can be reconfigured for each RF band by simply changing the resonant frequency of the load network. The frequency characteristics of the active-RC channel selection filter with an R-2R ladder is automatically tuned by a one-shot tuning circuit. The measured NF of the receiver implemented in a 0.18-μm CMOS process is 4.6–5.6 dB. [6]

Kyoohyun Lim, Sunki Min, Sanghoon Lee, Jaewoo Par, KisubKang,Hwahyeong Shin, Hyunchul Shim, Sechang Oh, Sungho Kim, Jongryul Lee, Changsik Yo and Kukjin Chun(2011) proposed a 2x2 MIMO Tri-Band Dual-Mode Direct-Conversion CMOS Transceiver for Worldwide WiMAX/WLAN Applications. This transceiver should cover the frequency bands of 2.3–2.7 GHz, 3.3–3.9 GHz, and 5.1–5.9 GHz while supporting multiple channel bandwidths such as 3.5, 4.3, 5, 7, 8.7, 10, 14. The result shows that the noise figure of the receiver is 3.6–4.2 for 2GHz,4.2–4.7 for 3 GHz, and 5.4–6.2 dB for 5 GHz band. Linear RX and TX signals path ensures Low EVM for wide dynamic range.[7]

Jin-Fa Chang, Yo-Sheng Lin, Jen-How Lee, and Chien-Chin Wang (2012) proposed a Low-Power 3.2~9.7GHz Ultra-Wideband Low Noise Amplifierwith Excellent Stop-band Rejection Using 0.18μm CMOS Technology. a passive band-pass filter is used to achieve a high stop band rejection and in output terminal of LNA we use an active notch filter. power consumed by this LNA is 4.68 mW. The measured result shows that S_{11} of 10~ 39.5 dB, S_{21} of 9.3±1.5 dB,average NF of 6 dB over the 3.2~9.7 GHz band.[8]

Zhang Men and Li Zhiqun (2012) proposed a differential low power low noise amplifier designed for the wireless sensor network(WSN) in a TSMC 0.18 μm RF CMOS process. A two-stage cross-coupling CG topology has been designed as the amplifier. The LNA has been fabricated for a frequency 2.44 GHz. The results show S_{21} is variable with high gain at 16.8 dB and low gain at 1 dB. The NF at high gain mode is 3.6 dB, the input referenced 1 dB compression point was about –8 dBm. The LNA consumed around 1.2 mA current from 1.8 V power supply. [9]

Jun-Da Chen (2013) proposed ultrawideband low-noise amplifier chip using TSMC 0.18 μm CMOS technology. They proposed a UWB low noise amplifier (LNA) for low-voltage and low-power application.This UWB LNA is designed based on a current-reused topology, and a simplified RLC circuit is used to achieve the input broadband matching. The measured results of the proposed LNA show $S_{21}$of 9 dB with the 3 dB band from 3 to 5.6 GHz. S_{11} less than −9dB is from 3 to 11GHz.S_{22} less than −8 dB is from 3 to 7.5 GHz.The noise figure 4.6–5.3 dB is from 3 to 5.6GHz. Input third-order intercept point (IIP3) of 2 dBm is at 5.3GHz. The dc power consumption of this LNA is 9mW under the supply of a 1V supply voltage. [10]

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Othman A.R, Pongot, Zakaria, Suaidi M.K, Hamidon A.H Bahagian Sumber Manusia(2013) proposed a low noise and high gain cascoded LNA amplifier. This LNA was designed and used inductive feedback and T- matching network consisting of lump reactive at the input and output of the LNA circuit. The cascoded LNA produced low noise figure of 0.83 dB with high gain of 26.26 dB. The S-parameter S_{11}, S_{22}, and S_{12} are of -11.05 dB, -10.5 dB and -30.92 dB respectively. The bandwidth measured is 1.56 GHz, while the input sensitivity is -82.6 dBm which is compliant WiMAX standards. [11]

Naveen Motamarri (2014) proposed two RF CMOS narrow band LNAs (cascode, differential) are designed. All the circuits operate with 1.8v supply voltage. In the circuit, Enhanced cascode LNA exhibits a gain of 26.88dB and NF of 2.55dB and the Differential LNA exhibits a gain of 32.71dB and NF of 2.66dB. The circuits are designed using cadence 0.18μm RF CMOS technology. [12]

Heba A. Shawkey (2014) proposed a low noise amplifier (LNA) for 3.5-4.5 GHz UWB frequency range. This LNA has S_{21} of 21.7 dB with 0.9dB ripples in the designed frequency range ,S_{11} and S_{22} are -8.5 and -11 dB respectively. This proposed LNA has a NF of 1.6 dB, IIP3 of -18 dBm, 1-dB compression point of -23 dBm and is designed at UMC 130nm CMOS technology and consumes 4.8mW for 1.2 V power supply. [13]

Hsuan-ling Kao, Bai-Hong Wei, and Yi-Chun Lee (2015) proposed an 3.5 GHz low noise amplifier that uses a two-stage configuration, using 0.35 μm AlGaN/GaN HEMT on silicon substrate technology. The first stage has a cascode topology to achieve high gain, better stability and well reverse isolation. The second stage has a RC-feedback topology for wideband matching. The T-matching network is used for broadband output matching. The result by their LNA shows a maximum gain of 14.4 dB, a minimum NF of 3.3 dB, and S_{11} and S_{22} greater than 10 dB. With good power-handling capabilities of GaN HEMT devices, the third-order input intercept point at 3.5 GHz is +2.5 dBm and the unit consumes 170 mW of power. [14]

Firmansyah Teguh, Supriyanto Supriyanto and Herudin (2016) proposed a LNA that has a center frequencies 0.95 GHz for GSM, 1.85 GHz for WCDMA, and 2.45 GHz for WLAN application.Advanced Design System (ADS) is used for simulation. If LNA at center frequency of 0.95 GHz ,the results of simulation are S_{11} =-31.351 dB,S_{22} =-26.004 dB,S_{21} = 19.084 dB,NF = 1.756 dB. At frequency of 1.85 GHz, S_{11}=-25.013 dB, S_{22} =-25.626 dB,S_{21} = 12.968 dB, NF = 1.995 dB. At center frequency of 2.45 GHz, S_{11}= -26.691 dB, S_{22} =-26.984 dB,S_{21} = 8.461 dB, NF = 2.991 dB. Results show that this LNA can operate in multiple frequency and its applications are GSM, WCDMA, and WLAN.[15]

Saurabh Pargaien, Abhishek Tomar and Ankur Bingh bist (2016) proposed a low power CMOS RF front-end LNA architecture, input matching with inductive source degeneration topology and current reused technique.This circuit provides performance from 3.34-3.92 GHz using a TSMC 0.18 μm CMOS process. The fully integrated LNA exhibits a gain of S_{11} is 17.74 dB, a noise figure less than 1dB from 1.4 GHz to 4.9 GHz, operating at a supply voltage of 1.8 V. The input return loss is –23.26 dB and output return loss is S_{22} -11.3 dB. [16]

Table 1.1 Target specifications of the LNA

Categories	Specifications
Noise figure	≤ 2 dB
S_{11}	≤ -10 dB
S_{22}	≤ -10 dB
IIP3	≤ -10 dBm
S_{21}	≥ 15 dB
S_{12}	≥ -20 dB
Stability factor	> 1
Input Impedance	50 Ω
Output Impedance	50 Ω

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